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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,453	08/28/2001	Fang-Cheng Chang	NTI-024	6364

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EXAMINER

MOHAMEDULLA, SALEHA R

ART UNIT	PAPER NUMBER
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1756

DATE MAILED: 04/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/941,453

Applicant(s)

CHANG ET AL.

Examiner

Saleha R. Mohamedulla

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 3/15/05.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12,48-52,55 and 56 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12,48-52,55 and 56 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 5/12/03; 12/9/02; 8/16/02; 3/19/01
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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DETAILED ACTION

Claims 1-12, 48-52, 55 and 56 are pending.

Information Disclosure Statement

1. References are crossed out in the IDS as they do not have reference date listed.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-12, 48-52, 55 and 56 are rejected under 35 U.S.C. 102(b) as being anticipated by US# 5,597,668 to Nowak et al.

Nowak teaches photomask generation. The planarity of the dielectric layer over a processing layer is increased by adjustments made to a mask generated for patterning the processing layer. Active circuitry lines are generated for the mask. Also, a fill pattern is generated for the mask. The fill pattern is placed in areas of the mask not filled by the active circuitry lines. The active circuitry lines are combined with the fill pattern to produce a final pattern for the mask. In one embodiment, the fill pattern is generated by first over-sizing the active circuitry lines to form a first pattern. The first pattern is inverted to produce a negative of the first pattern. The negative of the first pattern serves as a marker layer. In addition, a dummy fill pattern is generated. An intersection of the marker layer and the dummy fill pattern

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is performed to produce an unsized fill pattern. Areas which have widths smaller than a predetermined minimum width and areas which have heights smaller than a predetermined minimum height are eliminated from the unsized fill pattern to produce the final fill pattern. The union of the original active circuitry lines and the final fill pattern forms a composite pattern for the photomask. (Abstract). Therefore, Nowak also teaches determining the size of a feature. Nowak also teaches that planarization is achieved by placing a fill pattern on a mask for the layer that is to be planarized. In the preferred embodiment of the present invention, the fill pattern has the following characteristics. The fill pattern is made up of lines (called fill lines) and spaces comparable to those found on the circuit. Therefore, the spaces between geometries on the same layer throughout the circuit are fairly consistent. Design rules for circuitry are not violated. The fill lines are discontinuous at intervals to minimize the possibility of shorts. FIG. 1 is a flowchart which summarizes steps to generate a pattern filled mask in accordance with the preferred embodiment of the present invention. In a step 11, an active layer consisting of active circuitry lines is generated for a mask. This is done, for example, using generation software. The active circuitry lines determine the pattern of a mask resulting from implementation of a circuit design before a fill pattern is added. In a step 12, a marker layer is generated to mark areas on the mask to receive the fill pattern. The marker layer is generated by oversizing the active circuitry lines. For example, 0.75 microns is added in each direction to the width and to the height of each active circuitry line. After oversizing the active circuitry lines, the result is inverted to produce a negative of the pattern of the oversized active circuitry lines. The marker layer marks areas to be filled. In a step 13, a dummy fill pattern is generated, for example using a layout editor or an automated pattern generator. For example,

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the dummy fill pattern is composed of rectangles (fill lines) of predetermined length and width. For example, the width of each rectangle is one micron and the height of each rectangle is ten microns. The rectangles are repeated at a predetermined spacing. For example, the spacing between the rectangles is 0.75 microns in both the horizontal and the vertical directions. Other pattern shapes also may be used. For example, in an alternate embodiment, a herring bone pattern is used (col. 3, lines 5-20).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Saleha Mohamedulla whose telephone number is (571) 272-1387. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Saleha R. Mohamedulla
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Technology Center 1700
March 21, 2005